Your title of the talk at PIXEL 2010 Workshop

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Abstract

The CMS pixel barrel system will consist of three layers built of about 800 modules and half modules. One full module contains 66560 readout channels and the full pixel barrel system about 48 million channels. It is mandatory to test each channel for functionality, noise level, trimming mechanism, and bump bonding quality. Different methods to determine the bump bonding yield with electrical measurements have been developed. Measurements of several operational parameters are also included in the qualification procedure. Among them are pixel noise, gains and pedestals. Test and qualification procedures of the pixel barrel modules are described and some results are presented.

Keywords: Pixel detector, CMS

1. Introduction

The CMS pixel barrel module consists of a single sensor substrate with 16 front-end readout chips (ROC) bump-bonded to it and a hybrid circuit (HDI—high density interconnect) mounted on top of the sensor. Two thin strips of Si_3N_4 glued to the readout chips serve as a base to attach he module to the cooling frame. The whole pixel barrel detector will contain about 48 million readout channels. It is mandatory to test each channel for functionality, noise level, trimming mechanism, and bump bonding quality. The qualification process also includes the determination of the operational parameters (like trim bit settings, measurement of noise, gains and pedestals), a check of the sensor *I-V* dependence and a thermal cycling test. The time scale for the barrel detector construction is about one year. This implies a necessity to test four modules a day. To fulfill this time-constraint it is anticipated to use only tested components and perform a failure diagnostics in parallel with the qualification tests. Further details about the assembling procedure of the pixel modules can be found in [1].

2. Section 2 title

2.1. Subsection 2.1 title

To have identical conditions for all ROCs, the voltage of the analog part is set in the way that each ROC draws a current of 24mA. This is achieved by adjusting the Vana DAC. Starting from its default value, this DAC is increased (decreased) as long as the analog current is below (above) 24mA. The analog current is measured 100ms after setting the Vana DAC.

2.2. Subsection 2.2 title

To use the internal calibration signal for the further tests, its timing has to be brought into accordance with the trigger signal. The calibration signal of the ROC can be delayed with respect to the 40Mhz clock in steps of 1ns with the CalDel DAC. Furthermore the signal threshold, controlled by the VthrComp DAC, has to be tuned with the calibration signal. Since these two issues, the timing and the threshold, are strongly correlated, they are tuned in one step. The response of one pixel is scanned for over the whole VthrComp-CalDel parameter space. A typical result is shown in Fig. 1.

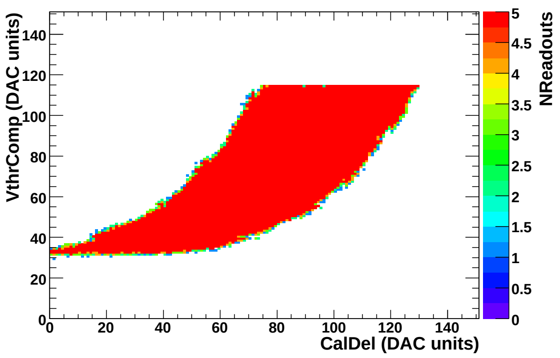

Figure 1: Signal region in the CalDel - VthrComp plane

3. Section 3 title

3.1. Subsection 3.1 title

The functionality of each pixel is checked by inducing a signal via an internal calibrate capacitance. First, it is tested that

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the masked (disabled) pixel does not respond if a calibrate signal is sent to it. Second, for the enabled pixel N calibrate signals are sent and the number of output signals is registered. The pixel is fully working if all signals were registered, the pixel is defective, if no output signal was registered at all. As a result of this test, a list of defective pixels is produced. Three modules have been tested so far and only 6 dead pixels have been found out of almost 200000 pixels.

3.2. Subsection 3.2 title

To fine tune the thresholds of the individual pixels, for each pixel unit cell four trim bits can be set. In this test, the functionality of these four trim bits is verified. The trimming mechanism is ineffective if all trim bits are turned on (trim value = 15). By turning off the trim bits the threshold of the pixel is lowered. In a first step the threshold of each pixel is determined in its untrimmed state. Afterwards each trim bit is turned off seperately and the threshold is measaured again. If no or only a very small difference in the threshold value is observed, the corresponding trim bit is defective. Fig. 2 shows the threshold difference for a ROC with one defective trim bit.

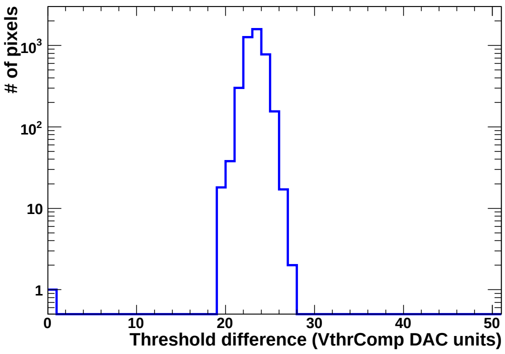


Figure 2: Threshold differences between trimmed and untrimmed state for all pixels on a ROC

3.3. Subsection 3.3 title

A bump bonding procedure has been developed at PSI (for details see [2]). A first test of its quality will be performed on the bare modules. But since bonds can be damaged during the module assembly it is mandatory to repeat the bump bonding test to identify pixels with missing or broken bumps on the fully equipped modules. To speed up and simplify the procedure several electrical methods without radioactive sources have been developed. Two of them rely on the fact, that if the ROC preamplifier is set close to saturation and a high leakage current is drawn through the bump, the preamplifier saturates. If the bump is missing, the preamplifier is not saturated. A high leakage current is generated with a light source (a lamp, for example) or with a positive bias. Any of these two methods can be used with bare modules when the sensor is not yet covered by the HDI.

For assembled modules a different method, called the 'modified external calibration' method is used. In the ROC the possibility to send a calibrate signal through the sensor is implemented [3].

4. Section 4 with multiple figures example

4.1. Subsection 4.1 with 2 figures example

The aim of the trim algorithm is to unify the physical thresholds of all pixels on a readout chip (ROC). To reach this goal, the following parameters can be adjusted. A global threshold can be set per ROC. To account for the pixel to pixel variations four trim bits can be set in each pixel unit cell. By setting these bits the threshold of the pixel is decreased. The strength of the correction is determined by the trim voltage, which can only be set per ROC. In Fig. 3(a) the threshold distribution is shown before the trimming procedure and in Fig. 3(b) the thresholds are shown for the trimmed ROC.

4.2. Subsection 4.2 with table example

Table 1 shows time taken by an individual test per ROC. The limiting factor is the data transfer between the testboard and the PC via an USB connection. Implementing simple data analysis functionalities directly in the FPGA on the testboard should considerably speed up all tests.

Table 1: Durations and numbers of triggers of the ROC test

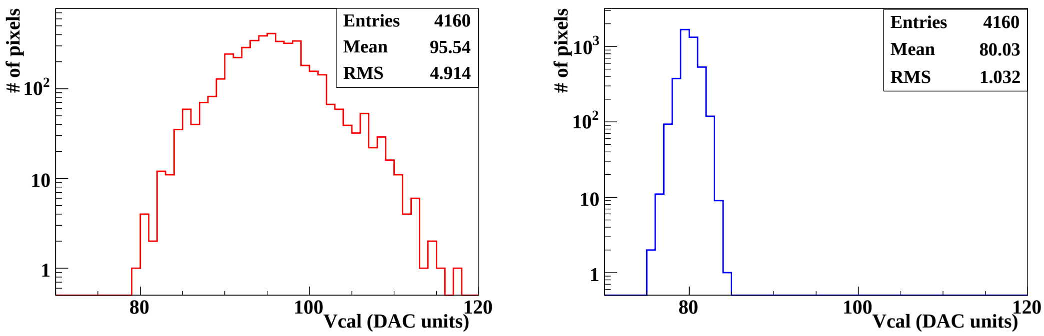
Test	Duration [s]	# triggers
Threshold / timing	12	5
Pixel test	1	10
Trim bits test	145	5
Bump-bonding test	80	10
Pixel address test	8	1
Noise (S-Curves)	210	50
Trimming	450	10
PH calibration	151	2

5. Section 5 title

Modules will be sorted in three or four quality classes. Those which pass the quality tests and have less than 1% of defective pixels will be qualified to be used in the pixel system. If the amount of defects is between 1% and 2%, modules may be considered as spare ones. If the number of defective pixels is more than 2%, modules will be rejected. In the three modules tested so far the maximum fraction of defective pixels is less than 10^{-4}.

6. Conclusion

In the coming years about 800 pixel modules will be assembled at PSI. Each of them should pass comprehensive tests and be qualified to be used in the construction of the CMS pixel



(a) (b)

Figure 3: Pixel threshold distribution for (a) untrimmed and (b) trimmed readout chip

barrel detector. A qualification procedure has been established to ensure a reliable and high-quality device. One of the most crucial tests is the bump bonding quality. Several procedures have been developed and validated. All of them provide consistent results. Another important procedure is the trimming of the ROCs. A sophisticated but fast algorithm has been developed to guarantee an excellent unification of the pixel thresholds down to 2%. The measurement of the pixel noise, gain and pedestal allows to set a module in the correct operational regime. I-V test and thermal cycling procedure ensure that modules can be operated under CMS conditions. The overall qualification procedure will be tuned and verified during the module pre-production period.

7. Acknowledgment

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References

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